UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,628	03/31/2004	Simon Knowles	66365-013	3813

7590 05/15/2006

MCDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
ZALEPA, GEORGE D	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,628	KNOWLES, SIMON	
	Examiner	Art Unit	
	George D. Zalepa	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-29 have been considered by the examiner.

Specification

2. The abstract of the disclosure is objected to because it exceeds 150 words. Correction is required. See MPEP § 608.01(b).

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Method and apparatus for separate control processing and datapath processing in a dual path processor with shared a load/store unit.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 27-29 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Furthermore, the computer program of claims 27 and 28 is not tangibly embodied on a computer-readable medium. As written, the computer program can be embodied on a non-statutory element such as a carrier wave or piece of paper. Furthermore, regarding claim 29, an instruction set does not constitute a computer readable medium as it can be represented on an intangible medium such as a technical manual.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3, 7-10, 12, 14, 16-19, 21, 23, 25, 26 and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Cousin (US Pat. No. 6,725,357).

7. Regarding **independent claim 1**,

8. Cousin discloses *a computer processor, the processor comprising: (a) a decode unit for decoding a stream of instruction packets from a memory* [see Cousin, Fig. 1, element 8 receiving instructions from element 2], *each instruction packet comprising a plurality of instructions* [see Cousin, Col. 3, lines 28-31; "...a number...of instructions..."]; *(b) a first processing channel* [see Cousin, Fig. 1, elements EXU3-5; Examiner's note: it is clear by elements D-IDQ and A-IDQ that there exists two separate channels.] *comprising a plurality of functional units* [see Cousin, Fig. 3, elements 143, 114] *and operable to perform control processing operations* [see Cousin, Col. 5, lines 17-26; "branch circuitry..." etc.]; *(c) a second processing channel* [see Cousin, Fig. 1, elements EXU1-2; Examiner's note: it is clear by elements D-IDQ and A-IDQ that there exists two separate channels.] *comprising a plurality of functional units* [see Cousin, Fig. 3, elements DU0-1] *and operable to perform data processing operations* [see Cousin, Col. 5, lines 17-18]; *wherein the decode unit is operable to receive an instruction packet* [see Cousin, Col. 3, lines 28-31] *and to detect* [see Cousin, Col. 4, lines 15-19] *if the instruction packet defines (i) a plurality of control instructions* [see Cousin, Col. 4, lines 19-22 "...address units...general unit..."] *or (ii) a plurality of instructions one or more of which is a data processing instruction* [see Cousin, Col. 4, lines 19-22 "...data units..."], *and wherein when the decode unit detects that the instruction packet comprises*

a plurality of control instructions said control instructions are supplied to the first processing channel for execution in program order [see Cousin, Col. 4, lines 15-19; Examiner's note: Cousin discloses a macro instruction being decoded into multiple micro operations and being routed to the appropriate channels (beginning with queues D-IDQ, A-IDQ). It is clear from all of the cites in this paragraph that Cousin distinguishes between control instructions (address and branch) and data instructions (essentially integer operations) as illustrated by the two separate datapaths shown in Fig. 3.].

9. Regarding **claim 2**,

10. Cousin discloses *the decode unit* [being] *operable to detect an instruction packet comprising three control instructions and control the control process to execute each of the three control instructions in the order in which they appear in the instruction packet* [see Cousin, Col. 4, lines 57-60; Examiner's note: Since the instruction in the cite contains eight instructions and up to eight can be control instructions, it is clear that Cousin discloses the ability to decode three control instructions.].

11. Regarding **claim 3**,

12. Cousin discloses *the decode unit* [being] *operable to detect an instruction packet containing a plurality of control instructions of equal length* [see Cousin, Fig. 2; Examiner's note: Fig. 2 shows macroinstructions containing microinstructions of equal length.].

13. Regarding **claim 7**,

14. Cousin discloses *the decode unit* [being] *operable to detect when there is at least one data processing instruction in the instruction packet and, in response thereto, to cause relevant data to be supplied to the data processing channel* [see Cousin, Col. 4, lines 15-19].

15. Regarding **claim 8**,

16. Cousin discloses *the decode unit* being *operable to detect that the instruction packet comprises at least one data processing instruction and a further instruction selected from one or more of: a memory access instruction; a control instruction; and a data processing instruction* [see Cousin, Col. 4, lines 15-

22; Examiner's note: It is clear from Fig. 3, that the "address unit" and "general unit" are designed to handle control instructions and memory accesses.].

17. Regarding **claim 9**,

18. Cousin discloses *at least one data processing instruction and said further instruction are executed simultaneously* [see Cousin, Col. 3, lines 10-13].

19. Regarding **claim 10**,

20. Cousin discloses *the second processing channel is dedicated to the performance of data processing operations* [see Cousin, Col. 3, lines 37-39] *and data processing instructions are provided in assembly language* [see Cousin, Col. 3, lines 15-18; Examiner's note: It would have been common at the time of invention to require the macro-instructions to be written in assembly code as was a common standard at the time of invention.].

21. Regarding **claim 12**,

22. Cousin discloses *the first processing channel* [comprising] *units selected from one or more of: a control register file* [see Cousin, Fig. 3, element 16; Col. 5, lines 40-44]*; a control execution unit* [see Cousin, Fig. 3, element 143]*; a branch execution unit* [see Cousin, Fig. 3, element 114] *and a load/store unit* [see Cousin, Fig. 3, element 150; Col. 3, line 60 to Col. 4, line 4].

23. Regarding **claim 14,**

24. Cousin discloses *the second processing channel* [comprising] *a data execution path including a fixed data execution unit* [see Cousin, Fig. 3, element 133].

25. Regarding **claim 16**,

26. Cousin discloses *the fixed data execution unit* [operating] *according to single instruction multiple data principles* [see Cousin, Fig. 3, elements 133; Examiner's note: Cousin discloses two execution units in parallel capable of acting in an SIMD manner.].

27. Regarding **claim 17**,

28. Cousin discloses *the data processing channel* [comprising] *one or more of a data register file* [see Cousin, Fig. 3, element 12] *and a load/store unit* [see Cousin, Fig. 3, element 150; Col. 3, line 60 to Col. 4, line 4].

29. Regarding **claim 18**,

30. Cousin discloses *a single load/store unit* [being] *accessed by both the control processing channel and the data processing channel through respective ports* [see Cousin, Fig. 3, element 150; Col. 3, line 60 to Col. 4, line 4].

31. Regarding **claim 19**,

32. Cousin discloses *the decode unit* [being] *operable to detect an instruction packet comprising at least one data processing instruction* [see Cousin, Col. 4, lines 15-22], *wherein the bit length of the at least one data processing instruction is between 30 and 38 bits* [see Cousin, Fig. 2, GP32 instruction and VLIW instruction].

33. Regarding **claim 21**,

34. Cousin discloses *the decode unit* [being] *operable to detect an instruction packet comprising a data processing operation and a memory access instruction* [see Cousin, Col. 4, lines 15-22; Examiner's note: It is clear from Fig. 3, that the "address unit" and "general unit" are designed to handle control instructions and memory accesses and "data unit" able to handle data processing instructions].

35. Regarding **claim 23**,

36. Cousin discloses *the decode unit* [being] *operable to detect an instruction packet comprising a data processing instruction and a control processing instruction* [see Cousin, Col. 4, lines 15-22; Examiner's note: It is clear from Fig. 3, that the "address unit" and "general unit" are designed to handle control instructions and memory accesses and "data unit" able to handle data processing instructions].

37. Regarding **claim 25**,

38. Regarding **independent claim 26**,

39. **Independent claim 26** is rejected as being the method performed by the apparatus in **independent claim 1.**

40. Regarding **independent claim 29,**

41. Cousin discloses *an instruction set for a computer including a first class of instruction packets each comprising a plurality of control instructions for execution sequentially* [see Cousin, Col. 4, lines 56-60; Examiner's note: Cousin allows for an instruction packet containing only control words.] *and a second class of instruction packets each comprising at least a data processing instruction and a further instruction for execution contemporaneously* [see Cousin, Col. 4, lines 56-60; Examiner's note: In the same cite, Cousin allows for differing types of operations ("...in each μ slot 0 and μ slot 1 of either the data units DU0 and DU1 or the address units AU0 and AU1/general unit GU.")], *said further instruction being selected from one or more of: a memory access instruction; a control instruction; and a data processing instruction* [see Cousin, Col. 4, lines 15-22; Examiner's note: It is clear from Fig. 3, that the "address unit" and "general unit" are designed to handle control instructions and memory accesses and "data unit" able to handle data processing instructions. With regard to Col. 4, lines 56-60, since an instruction packet can send instructions to each of these units simultaneously, it stands that there can be all three operations in one packet.].

Claim Rejections - 35 USC § 103

42. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

43. Claims 4-5, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cousin in view of Takayama et al (US Pat. No. 6,880,150; herein referred to as Takayama.).

44. Regarding **claim 4**,

45. Cousin discloses the limitations as stated in **claim 3**.

46. Cousin does not disclose detecting *within an instruction packet a control instruction of a bit length between 18 and 24 bits.*

47. Takayama discloses detecting *within an instruction packet a control instruction of a bit length between 18 and 24 bits* [see Takayama, Col. 13, lines 29-33].

48. The advantage of using control instructions that are between 18 and 24 bits in length (21 bits as disclosed by Takayama) would have been to allow control instructions to be executed even when other operations are performed in units of an integer number of bytes [see Takayama, Col. 2, lines 9-13]. This advantage is desirable, as it would have increased execution speed of control instructions and thus the entire system. This advantage would have motivated one of ordinary skill in the art to modify the instruction set to accommodate a 21-bit control instruction as disclosed by Takayama within the processor disclosed by Cousin.

49. Regarding **claim 5**,

50. Cousin and Takayama disclose the limitations as stated in **claim 4**.

51. Takayama further discloses detecting *within an instruction packet a plurality of control instructions each having a bit length of 21 bits* [see Takayama, Col. 13, lines 29-33].

52. The advantage of using control instructions that are 21-bits in length would have been to allow control instructions to be executed even when other operations are performed in units of an integer number of bytes [see Takayama, Col. 2, lines 9-13]. This advantage is desirable, as it would have increased execution speed of control instructions and thus the entire system. This advantage would have motivated one of ordinary skill in the art to modify the instruction set to accommodate a 21-bit control instruction as disclosed by Takayama within the processor disclosed by Cousin.

53. Regarding **claim 11**,

54. Cousin disclose the limitations as stated in **independent claim 1**.

55. Cousin does not disclose *control processing operations* [being] *performed on operands up to a first predetermined bit width and the data processing operations* [being] *performed on data up to a second pre-determined bit width, the second pre-determined bit width being larger than the first pre-determined bit width.*

56. Takayama discloses *control processing operations* [being] *performed on operands up to a first predetermined bit width and the data processing operations* [being] *performed on data up to a second pre-determined bit width, the second pre-determined bit width being larger than the first pre-determined bit width* [see Takayama, Col. 13, lines 29-33; Examiner's note: Use of 21-bit and 42-bit instructions.].

57. The advantage of using control instructions that are 21-bits in length would have been to allow control instructions to be executed even when other operations are performed in units of an integer number of bytes [see Takayama, Col. 2, lines 9-13]. This advantage is desirable, as it would have increased execution speed of control instructions and thus the entire system. This advantage would have motivated one of ordinary skill in the art to modify the instruction set to accommodate a 21-bit control instruction as disclosed by Takayama within the processor disclosed by Cousin.

58. Claims 6, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cousin.

59. Regarding **claim 6**,

60. Cousin discloses the limitations as stated in **independent claim 1**.

61. Cousin does not explicitly disclose *the decode unit* [being] *operable to receive and decode instruction packets of a bit length of 64 bits.*

62. However, it would have been obvious to one of ordinary skill in the art at the time of invention that the length of the instruction packed could be modified to allow for a more standard length depending on which instruction set architecture is to be used, such as the 64-bit IA-64 ISA. Furthermore, Cousin does not limit the size of a packet as the only criterion for decoding is that the instruction be divisible by

two or four. Thus it is clear that the size of an instruction is not the main focal point stressed by Cousin and therefore could be tailored to fit a certain instruction set more suited to a particular application.

63. Regarding **claim 22,**

64. Cousin discloses the limitations as stated in **independent claim 1**.

65. Cousin does not explicitly disclose *the bit length of said memory access instruction* [being] *28 bits.*

66. However, it would have been obvious to one of ordinary skill in the art at the time of invention that the bit lengths of instructions disclosed in Cousin are of little significance and the primary concern set forth by Cousin is merely the alignment of instructions within the packet (Fig. 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a smaller instruction size than 32 bits in the invention disclosed by Cousin with the goals of either saving space or adapting the invention to a customized standard. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of invention that the size of an individual word is of no consequence given the words are still aligned properly as disclosed by Cousin.

67. Regarding **claim 24,**

68. Cousin discloses the limitations as stated in **independent claim 1**.

69. Cousin does not explicitly disclose the *decode unit* [being] *operable to detect a control processing instruction in C code or variant thereof.*

70. However, it would have been obvious to one of ordinary skill in the art at the time of invention to enable a processor to support higher level languages, such as C, as the languages are easier to develop code in and are more commonly used to develop code in. Therefore, it would have been obvious to allow a user to utilize an easier language such as C to code control instructions.

71. Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cousin in view of DeHon et al. (US Pat. No. 5,956,518; herein referred to as "DeHon".).

72. Regarding **claim 13**,

73. Cousin disclose the limitations as stated in **independent claim 1**.

74. Cousin do not disclose *the second processing channel* [comprising] *a data execution path including a configurable data execution unit.*

75. DeHon does disclose *a data execution path including a configurable data execution unit* [see DeHon, Col. 5, lines 23-26].

76. The advantage of using a configurable data execution unit in place of a fixed execution unit would have been to allow greater flexibility for processing ability, as would have been known to one of ordinary skill in the art at the time of invention [see DeHon, Col. 1, lines 41-47]. The idea of utilizing a programmable chip, such as an FPGA, would have been very common at the time of invention and furthermore, the benefits of reprogrammable processing to implement a variety of application specific functions would have been common at the time of invention. The advantage of using a configurable execution unit would have been to allow for a seemingly infinite amount of processing capability with a relatively low amount of chip space needed, as the programmable units could be reprogrammed if necessary. This advantage would have motivated one of ordinary skill in the art to utilize the programmable datapath ideas disclosed by DeHon in the invention disclosed by Cousin for the purpose of providing a more robust processor.

77. Regarding **claim 15**,

78. McMahan and DeHon disclose the limitations as stated in **claim 14**.

79. McMahan does not disclose *the configurable data execution unit* [operating] *according to single instruction multiple data principles.*

80. DeHon does disclose *the configurable data execution unit* [operating] *according to single instruction multiple data principles* [see DeHon, Col. 5, lines 23-26].

81. The advantage of using an SIMD architecture as disclosed by DeHon would have been to enable the processor disclosed by Cousin to more efficiently handle large quantities of data in parallel. Given the parallel nature of the processor disclosed by Cousin, it would have been obvious to one of ordinary skill in the art at the time of invention that an SIMD architecture would have further increased the data processing capabilities of a data processing execution unit. Furthermore, with the increasing use of DSP processors, a move to an SIMD architecture in the data execution channel would have enable one to utilize the processor disclosed by Cousin in a competitive nature with other DSP processors utilizing an SIMD architecture. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use an SIMD architecture disclosed by DeHon within the data processing channel disclosed by Cousin for the purpose of increasing data throughput in an environment operating on large quantities of data.

82. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cousin in view of Simonen et al ("Variable Length Instruction Compression for Area Minimization", Piia Simonen, Ilkka Saastamoinen, Jari Nurmi, 2003, IEEE; herein referred to as "Simonen".).

83. Regarding **claim 20**,

84. Cousin disclose the limitations as stated in **claim 19**.

85. Cousin further disclose *the decode unit* [being] *operable to detect an instruction packet comprising at least one data processing instruction.*

86. McMahan does not disclose *a bit length of the at least one data processing instruction is 34 bits.*

87. Simonen does disclose *a bit length of the at least one data processing instruction is 34 bits* [see Simonen, Section 3.1 ("Control Bits"), lines 3-4.].

88. The advantage of utilizing a 34-bit data processing instruction would have been to reduce the amount of space needed to implement certain data processing instructions [see Simonen, section 1, lines 1-4; section 3.1, lines 5-7]. This advantage is desirable in the invention disclosed by Cousin as it would

have increased the overall throughput of a processor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize the 34-bit control instructions as disclosed by Simonen with the goal of reducing processor execution time in the invention disclosed by Cousin.

89. Claims 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cousin in view of Tanenbaum (Andrew S. Tanenbaum. Structured Computer Organization, 1984. Pg. 10-11; herein referred to as "Tanenbaum").

90. Regarding **claim 27**,

91. Cousin discloses the limitations as stated in **independent claim 26**.

92. Cousin does not disclose the method of claim 26 being embodied on a computer program product comprising program code.

93. However, Tanenbaum discloses that "hardware and software are logically equivalent" and that any hardware apparatus can be simulated in software [see Tanenbaum, p. 11, lines 11-13]. The advantage of implementing the method disclosed within claim 18 within a machine-accessible medium would have been to exploit the advantages of software-based approaches such as cost or ease of upgrading [see Tanenbaum, p. 11, lines 13-15]. This advantage would have motivated one of ordinary skill in the art to implement the method disclosed in the body of claim 27 in software as opposed to in hardware.

94. Regarding **claim 28**,

95. Cousin discloses the limitations as stated in **independent claim 26**.

96. Cousin does not disclose the method of claim 26 being embodied in a program code.

97. However, Tanenbaum discloses that "hardware and software are logically equivalent" and that any hardware apparatus can be simulated in software [see Tanenbaum, p. 11, lines 11-13]. The advantage of implementing the method disclosed within claim 18 within a machine-accessible medium would have been to exploit the advantages of software-based approaches such as cost or ease of

upgrading [see Tanenbaum, p. 11, lines 13-15]. This advantage would have motivated one of ordinary skill in the art to implement the method disclosed in the body of claim 28 in software as opposed to in hardware.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George D. Zalepa whose telephone number is (571) 272-6754. The examiner can normally be reached on Monday-Friday (alt. Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

George Zalepa
Examiner
Art Unit 2183
Randolph 2E74
Phone: (571)272-6754

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100